The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ALAN BERENBAUM, NEVIN HEINTZE, TOR JEREMIASSEN and STEFANOS KAXIRAS

Appeal No. 2005-0443
Application 09/538,670

ON BRIEF

Before JERRY SMITH, BARRETT, and RUGGIERO, Administrative Patent Judges.

JERRY SMITH, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal under 35 U.S.C. § 134 from the examiner's rejection of claims 1-16, which constitute all the claims in the application.

The disclosed invention pertains to a multithreaded very large instruction word (VLIW) processor.

Representative claim 1 is reproduced as follows:

1. A multithreaded very large instruction word processor, comprising:

a plurality of functional units for executing a plurality of instructions from an instruction stream having a plurality of threads, said threads having a priority; and

an allocator that selects instructions from said instruction stream and forwards said instructions to said plurality of functional units, said allocator selecting said instructions based on said thread priority and independently allocating said functional units to any thread in said multithreaded instruction stream.

The examiner relies on the following reference:

Chung et al. (Chung) 5,404,469 Apr. 4, 1995

Claims 1-16 stand rejected under 35 U.S.C. § 102(b) as being anticipated by the disclosure of Chung.

Rather than repeat the arguments of appellants or the examiner, we make reference to the briefs and the answer for the respective details thereof.

OPINION

We have carefully considered the subject matter on appeal, the rejection advanced by the examiner and the evidence of anticipation relied upon by the examiner as support for the rejection. We have, likewise, reviewed and taken into

consideration, in reaching our decision, the appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejection and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the disclosure of Chung does not fully meet the invention as set forth in claims 1-16. Accordingly, we reverse.

Appellants have indicated that for purposes of this appeal the claims will all stand or fall together as a single group [brief, page 2]. Consistent with this indication appellants have made no separate arguments with respect to any of the claims on appeal. Accordingly, all the claims before us will stand or fall together. Note In re King, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983). Therefore, we will consider the rejection against independent claim 1 as representative of all the claims on appeal.

Anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital

Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

The examiner has indicated how he finds the claimed invention to be fully met by the disclosure of Chung [answer, pages 2-3]. With respect to representative claim 1, appellants argue that although Chung teaches that instructions are allocated to functional units, the allocation of instructions (functional units?) is not done independently of the type of instruction as claimed. Specifically, appellants argue that each of the functional units in Chung is dedicated to executing particular types of instructions and, therefore, each functional unit can only be allocated to a thread that has an instruction ready for execution wherein the instruction type matches the capability of the functional unit. Thus, appellants assert that the allocation of functional units in Chung is dependent on the type of instructions ready for execution within each thread rather than independently as claimed [brief, page 3].

The examiner responds that the allocation of instructions independently of the type of instruction ready for execution within each thread is not the disclosed or claimed invention.

Rather, the examiner points out that the disclosed invention is that the functional units are independently allocated to the threads, not that the allocation is independent of the instruction type. The examiner notes that claims 5-7 indicate that instructions are allocated based on the availability of the functional units and that instructions are allocated only if the required functional unit is available. The examiner notes that identifying the required functional unit is conventionally done on the basis of the type of instruction [answer, pages 3-4].

Appellants respond that the claimed invention requires that the allocation be independent of the instruction type. Appellants also respond that claims 5-7 merely recite that functional units must be available before they can be allocated to a thread of an instruction stream. Appellants also note that identifying a functional unit during allocation does not mean that the functional units are limited to specific operations [reply brief, pages 2-3].

We will not sustain the examiner's rejection of representative claim 1 for essentially the reasons argued by appellants in the answer. The claim recites "independently allocating said functional units to any thread in said multithreaded instruction stream" [emphasis added]. We interpret

this recitation as requiring that each functional unit must be capable of receiving any instruction thread. In other words, the functional units must essentially be identical full function units so that they can be used regardless of the type of instruction. As argued by appellants, the functional units disclosed in Chung are limited units based on the type of instruction. Specifically, function units FU1-FU4 in Chung are respectively an arithmetic unit, a logic unit, a load/store unit, and a branch unit [column 7, lines 43-46]. Therefore, functional unit FU1, for example, cannot be allocated a load or branch instruction and consequently, functional unit FU1 cannot be allocated to any instruction as claimed. Similar constraints apply to the other functional units. Thus, the fact that the functional units in Chung are limited in operation precludes their allocation being independent of the thread in a multithreaded instruction stream as claimed.

Since each of independent claims 5, 9, 12, 15 and 16 contain recitations similar to independent claim 1, we do not sustain the examiner's rejection of any of these claims for the same reasons discussed above with respect to claim 1. Therefore, the decision of the examiner rejecting claims 1-16 is reversed.

As noted above, Chung fails to anticipate the claimed invention because the functional units are not capable of being independently allocated as claimed. Nevertheless, we note that appellants' admitted prior art [Figures 1, 2, 4 and 5] may suggest that it was well known in this art to use a plurality of identical functional units in parallel in order to perform computer processing faster. If the limited functional units of Chung were replaced with identical full function units as used in the admitted prior art, it appears that the claimed invention on appeal would be met. Whether or not it would have been obvious to modify the processor of Chung to use identical functional units is a question of fact that has not been argued on this record. We leave it to the examiner to consider whether an evidentiary record to support a rejection of these claims on

appeal can be made using Chung, the admitted prior art submitted by appellants, or on any other prior art.

REVERSED

JERRY SMITH)
Administrative Patent Judge)
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LEE E. BARRETT) BOARD OF PATENT
Administrative Patent Judge) APPEALS AND
) INTERFERENCES
)
JOSEPH F. RUGGIERO)
Administrative Patent Judge)

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JS:dym

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